Ultra-Low Noise, 3.5 MHz Zero Drift, RRIO Op-amps

Features

- Supply Voltage: 1.8 V to 5.5 V
- Low Offset Voltage: 5 μV (max)
- Zero Drift: 0.05 μV/°C (max)
- No 1/f Noise Corner Down to 0.1Hz
  - Input Noise Voltage: 15 nV/√Hz at 1 kHz
  - 0.1 Hz to 10 Hz Voltage Noise: 350 nV_{PP}
- Slew Rate: 2.5 V/μs
- Bandwidth: 3.5 MHz
- Low Supply Current: 550 μA per Amplifier
- Low Input Bias Current: 50 pA Typical
- Rail-to-Rail Output Voltage Range
- High gain, CMRR, PSRR: 130 dB
- 7 kV HBM ESD Rating
- −40°C to 125°C Operation Range

Applications

- Medical Instrumentation
- Temperature Measurements
- Precision current sensing
- Precision Low Drift, Low Frequency ADC Drivers
- Process Control Systems
- Precision Voltage Reference Buffers

Description

The family of the amplifier are single/dual/quad chopper-stabilized zero-drift operational amplifiers optimized for single or dual supply operation from 1.8 V to 5.5 V and ±0.9 V to ±2.75 V. TP555X features very low input offset voltage and low noise with no 1/f noise corner down to 0.1 Hz. The TP555X is designed to have ultra-low offset voltage and offset temperature drift, wide gain bandwidth and rail-to-rail input/output swing while minimizing power consumption.

This TP555X family can provide very low offset voltage (max 5 μV) and near-zero drift over time and temperature with excellent CMRR and PSRR.

The TP5551 (single version) is available in SOT23-5, and SOP8 packages. The TP5552 (dual version) is offered in MOSP8, SOP8 package. The TP5554 (quad version) is available in TSSOP14, SOP14 package. All versions are specified for operation from −40°C to 125°C.

Typical Application Circuit

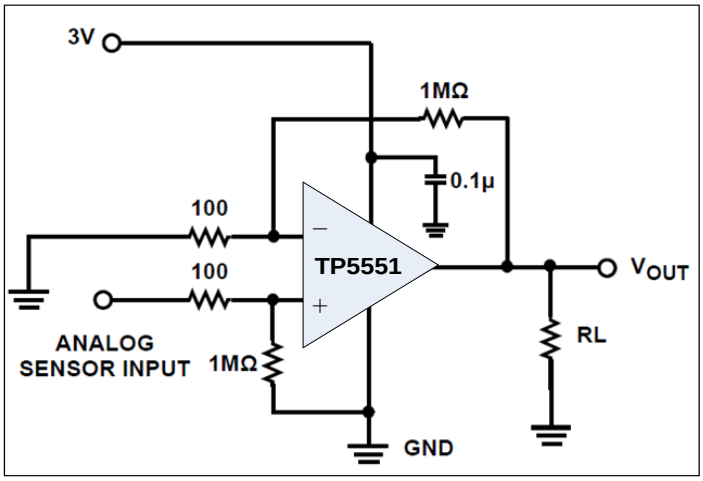


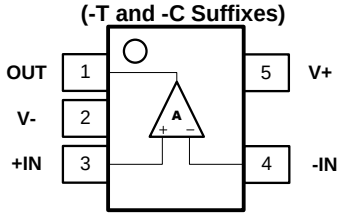
Table of Contents

Revision History

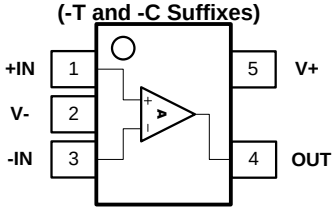
Date	Revision	Notes
2018-08-30	Rev.B.0	Updated Full Temperature Specification
2020-05-25	Rev.B.1	Updated Specification of PSRR: 25°C: min 95 → min 110; −40°C to 125°C: min 85 → min 105
2022-02-17	Rev.B.2	Updated Format of Document
2022-03-19	Rev.B.3	Updated Tape and Reel Information
2023-07-08	Rev.B.4	The following updates are all about the new datasheet formats or typo, the actual product remains unchanged. Updated to new format of package dimensions and tape and reel information.

Pin Configuration and Functions

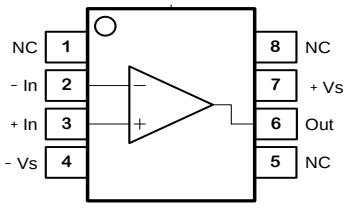
TP5551
SOT23-5/SC70-5
(-T and -C Suffixes)



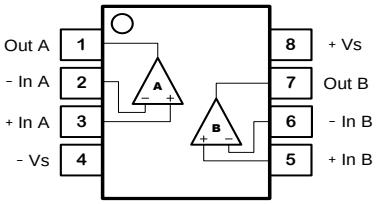
TP5551U
SOT23-5/SC70-5
(-T and -C Suffixes)



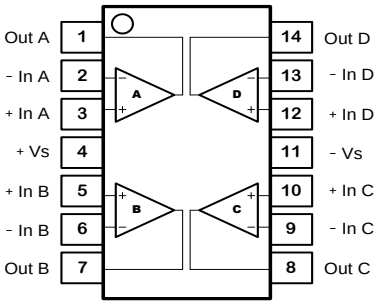
TP5551
8-Pin SOIC
(-S Suffix)



TP5552
8-Pin SOIC/MSOP
(-S and -V Suffixes)



TP5554
14-Pin SOIC/TSSOP
(-S and -T Suffixes)



Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Supply Voltage			7	V
Input Voltage		(V^-) − 0.3	(V^+) + 0.3	V
Input Current: +IN, −IN (2)			±20	mA
Output Current: OUT			±60	mA
Output Short-Circuit Duration (3)			Indefinite	
Current ar Supply Pins			±50	mA
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Electrical Characteristics

All test conditions: V_{DD} = 5 V, R_L = 10 K, V_{CM} = V_{DD}/2, T_A = +27°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range		1.8		5.5	V
I_Q	Quiescent current per amplifier	TP5551		1200	1400	μA
		TP5551, T_A = −40°C to 85°C			1600	μA
		TP5551, T_A = −40°C to 125°C			1750	μA
		TP5552/4		550	950	μA
		TP5552/4, T_A = −40°C to 85°C			1150	μA
		TP5552/4, T_A = −40°C to 125°C			1300	μA
V_{OS}	input Offset Voltage			±1	±5	μV
		T_A = −40°C to 125°C			±10	μV
dVos/dT	vs temperature			0.008	0.05	μV/°C
PSRR	vs power supply	Vs = +1.8 V to +5.5 V	110	130		dB
		Vs = +1.8 V to +5.5 V, T_A = −40°C to 125°C	105			
V_N (p-p)	input voltage noise, f = 0.01 Hz to 1 Hz			0.1		$μV_{pp}$
	input voltage noise, f = 0.1 Hz to 10 Hz			0.35		$μV_{pp}$
V_N	Input voltage noise density, f = 1 kHz			15		nV/√Hz
C_{IN}	Input capacitor Differential			3		pF
	Input capacitor Common-Mode			2		pF
I_B	Input Current			±50		pA
	Over temperature			±200		pA
I_{OS}	Input offset current			±100		pA
V_{CM}	Common-mode voltage range		(V^-) − 0.1		(V^+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5 V, V_{CM} = 0.5 V to 4.5 V	110	130		dB
		V_S = 5 V, V_{CM} = 0 V to 5 V	100	120		dB
		V_S = 5 V, V_{CM} = 0 V to 5 V, T_A = −40°C to 125°C	90			dB
V_O	Output Voltage Swing from rail	R_L = 10 kΩ		10	25	mV
		R_L = 10 kΩ, T_A = −40°C to 125°C			30	mV
I_{SC}	Short-circuit current			±50		mA
GBW	Unity Gain Bandwidth	C_L = 100 pF		3.5		MHz
SR	Slew rate	G = +1, C_L = 100 pF		2.5		V/μs

Electrical Characteristics (Continued)

All test conditions: V_{DD} = 5 V, R_L = 10 K, V_{CM} = V_{DD}/2, T_A = +27°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{or}	Overload recovery time	G = −10		35		μs
t_s	Settling time to 0.01%	C_L = 100 pF		20		μs
A_{VO}	Open-Loop Voltage Gain	(V_-) + 100 mV < V_O < (V_+) − 100 mV, R_L = 100 kΩ	100	120		dB
		(V_-) +100 mV < V_O < (V_+) – 100 mV, R_L = 100 kΩ, T_A = −40°C to 125°C	90			dB
θ_{JA}	Thermal Resistance Junction to Ambient	SOT23-5		200		°C/W
		MSOP8		210		
		SOP8		158		
		SOP14		83		
		TSSOP14		100		

Typical Performance Characteristics

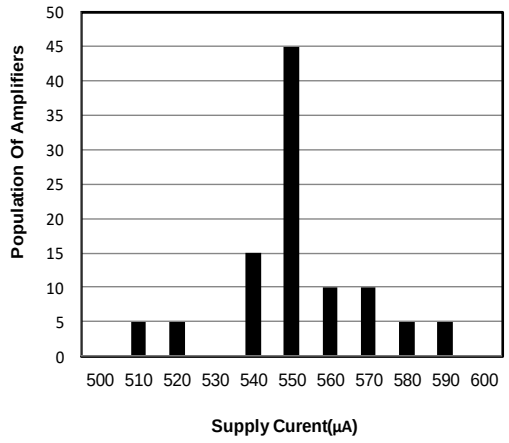


Figure 1. Supply Current Distribution

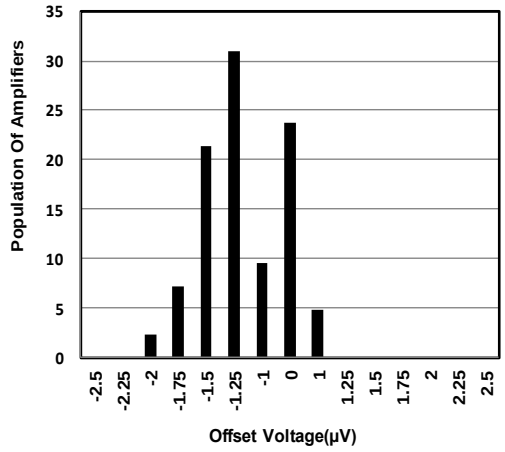


Figure 2. Offset Voltage Distribution

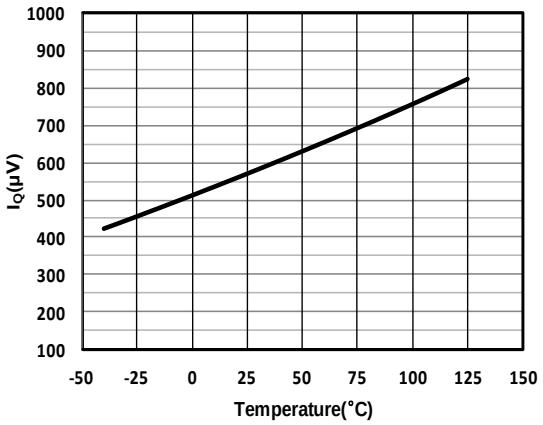


Figure 3. Quiescent Current vs Temperature

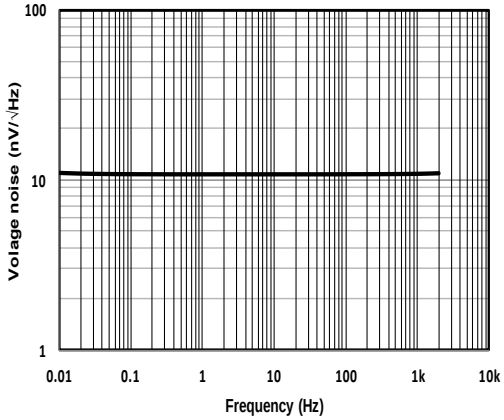


Figure 4. Voltage Noise Spectral Density vs Frequency

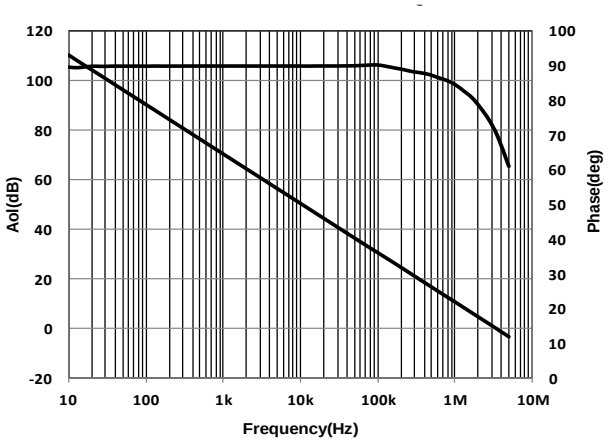


Figure 5. Open-Loop Gain vs Frequency

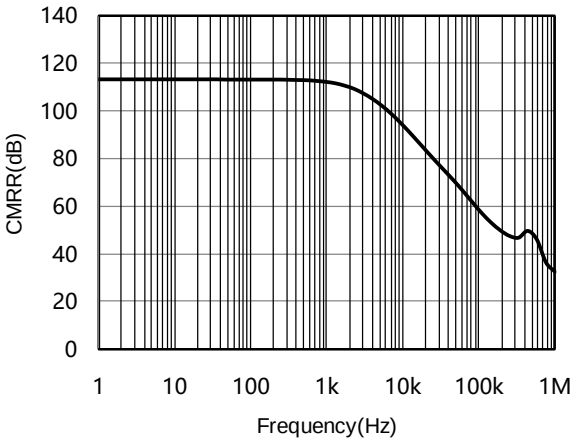


Figure 6. CMRR vs Frequency

Typical Performance Characteristics (Continued)

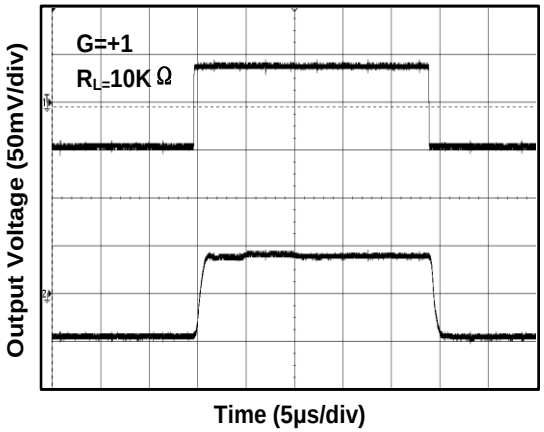


Figure 7. Small-Scale Step Response

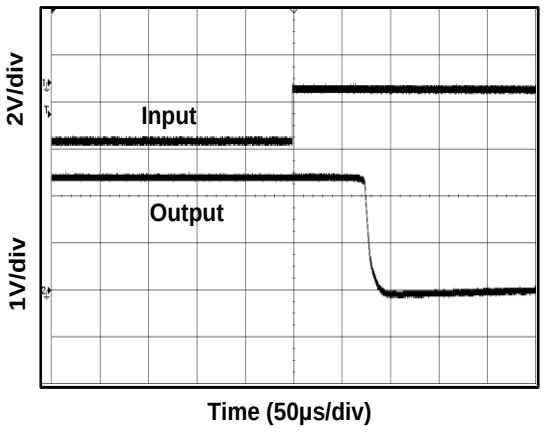


Figure 8. Positive Over-Voltage Recovery

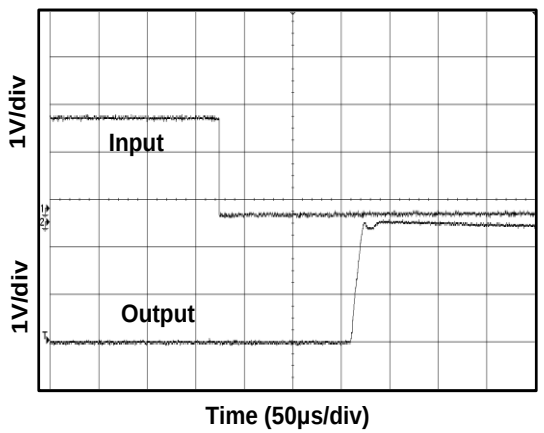


Figure 9 Negative Over-Voltage Recovery

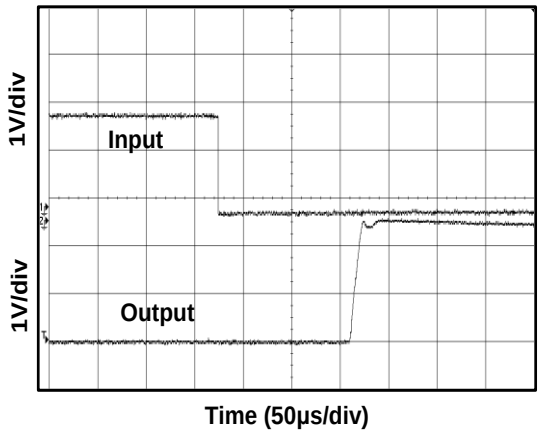


Figure 10 Large-Scale Step Response

Detailed Description

Overview

The TP5551/2/4 op amps are zero drift, rail-to-rail operation amplifiers that can be run from a single-supply voltage. They use an auto-calibration technique with a time-continuous 3.5 MHz op amp in the signal path while consuming only 550 μA of supply current per channel. This amplifier is zero-corrected with an 150 kHz clock. Upon power-up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

Functional Block Diagram

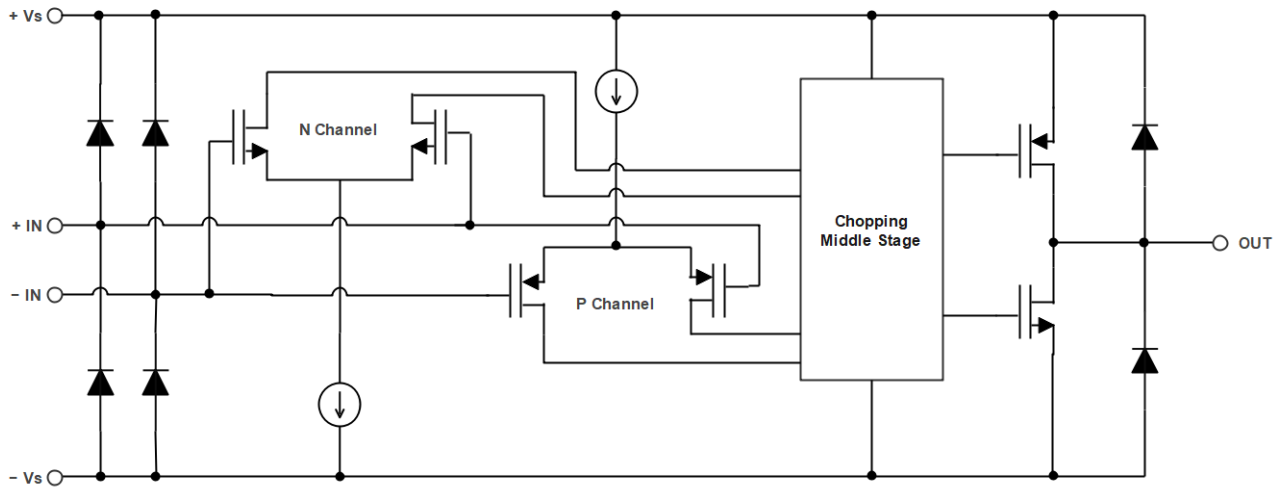


Figure 11 Functional Block Diagram

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

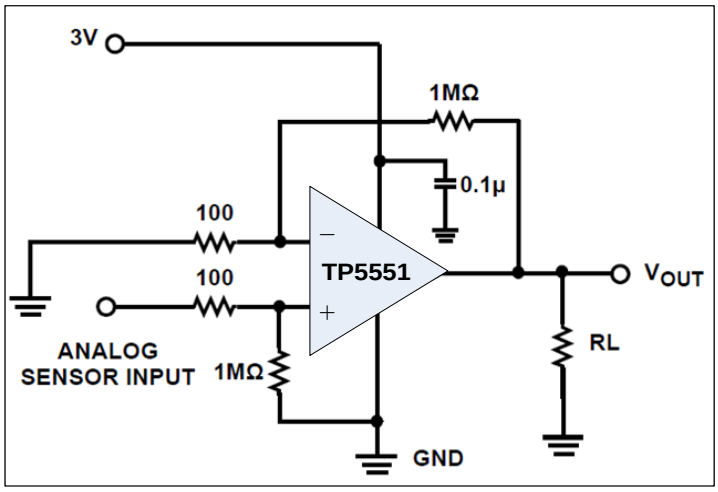


Figure 12. Single Supply, High Gain Amplifier, AV = 10,000 V/V

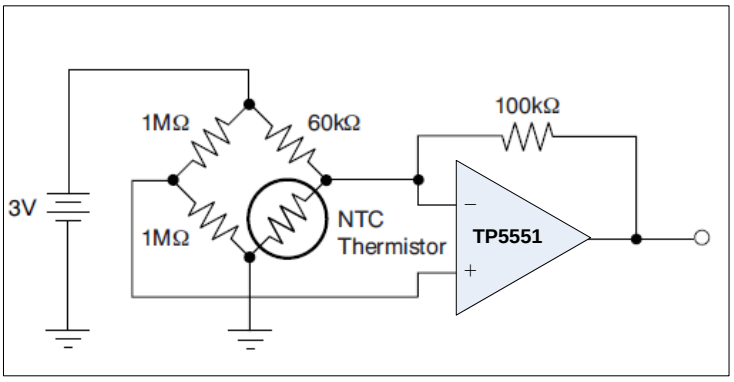


Figure 13 Thermistor Measurement

Application Information

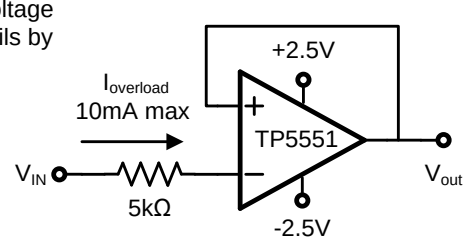
Rail-To-Rail Input And Output

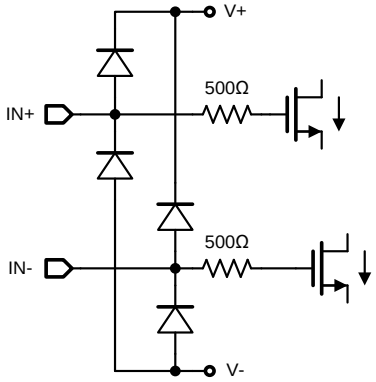
The TP5551/2/4 feature rail-to-rail input and output with a supply voltage from 1.8 V to 5.5 V. This allows the amplifier inputs to have a wide common mode range (50 mV beyond supply rails) while maintaining high CMRR (120 dB) and maximizes the signal to noise ratio of the amplifier by having the V_{OH} and V_{OL} levels be at the V+ and V- rails, respectively.

Input Protection

The TP5551/2/4 have internal ESD protection diodes that are connect between the inputs and supply rail. When either input exceeds one of the supply rails by more than 300 mV, the ESD diodes become forward biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device. Thus an external series resistor must be used to ensure the input currents never exceed 10 mA.

Current-limiting resistor required if input voltage exceeds supply rails by >0.5V.





INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

Low Input Referred Noise

Flicker noise, as known as 1/f noise, is inherent in semiconductor devices and increases as frequency decreases. So at lower frequencies, flicker noise dominates, causing higher degrees of error for sub-Hertz frequencies or dc precision application.

The TP5551/2/4 amplifiers are chopper stabilized amplifiers, the flicker noise is reduced greatly because of this technique. This reduction in 1/f noise allows the TP5551/2/4 to have much lower noise at dc and low frequency compared to standard low noise amplifier.

Residual voltage ripple

The chopping technique can be used in amplifier design due to the internal notch filter. Although the chopping related voltage ripple is suppressed, higher noise spectrum exists at the chopping frequency and its harmonics due to residual ripple.

So if the frequency of input signal is nearby the chopping frequency, the signal maybe interfered by the residue ripple. To further suppress the noise at the chopping frequency, it is recommended that a post filter be placed at the output of the amplifier.

Broad Band and External Resistor Noise Considerations

The total broadband noise output from any amplifier is primarily a function of three types of noise: input voltage noise from the amplifier, input current noise from the amplifier, and thermal (Johnson) noise from the external resistors used around the amplifier. These noise sources are not correlated with each other and their combined noise can be summed in a root sum squared manner. The full equation is given as:

$$e_n\ total = [e_n^2 + 4kTR_s + (i_n \times R_s)^2]^{1/2} \qquad (1)$$

Where:

e_n = the input voltage noise density of the amplifier.

I_n = the input current noise of the amplifier.

R_S = source resistance connected to the noninverting terminal.

K = Boltzmann's constant (1.38 x 10^{-23}J/K).

T = ambient temperature in Kelvin (K).

The total equivalent rms noise over a specific bandwidth is expressed as:

$$e_{n,rms} = e_n\ total \times \sqrt{BW} \qquad (2)$$

The input voltage noise density (en) of the TP555x is 55 nV/√Hz, and the input current noise can be neglected. When the source resistance is 190 kΩ, the voltage noise contribution from the source resistor and the amplifier are equal. With source resistance greater than 190 kΩ, the overall noise of the system is dominated by the Johnson noise of the resistor itself.

High Source Impedance Application

The TP5551/2/4 uses switches at the chopper amplifier input, the input signal is chopped at 125 kHz to reduce input offset voltage down to 10 μV. The dynamic behavior of these switches induces a charge injection current to the input terminals of the amplifier. The charge injection current has a DC path to ground through the resistances seen at the input terminals of the amplifier. Higher input impedance causes an apparent shift in the input bias current of the amplifier.

Because the chopper amplifier has charge injection currents at each terminal, the input offset current will be larger than standard amplifiers. The I_{OS} of TP5551/2/4 are 150 pA under the typical condition. So the input impedance should be balanced across each input. The input impedance of the amplifier should be matched between the IN+ and IN− terminals to minimize the total input offset current. Input offset currents show up as an additional output offset voltage, as shown in the following equation:

$$v_{os,total} = v_{os} - R_f \times I_{os} \qquad (3)$$

For a gain configure using 1MΩ feedback resistor, a 150pA total input offset current will have an additional output offset voltage of 0.15 mV. By keeping the input impedance low and balanced across the amplifier inputs, the input offset current effect will be suppressed efficiently.

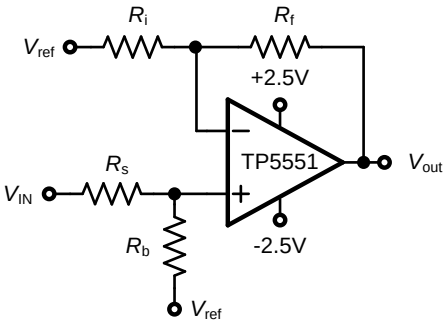


Figure 14 Circuit Implication for reducing Input offset current effect

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. It is recommended to use multi-layer PCB layout and route the OPA's −IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown below for

Inverting

Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

a) Connect the non-inverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.

b) Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

a) Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the op-amp (e.g., $V_{DD}/2$ or ground).

b) Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.

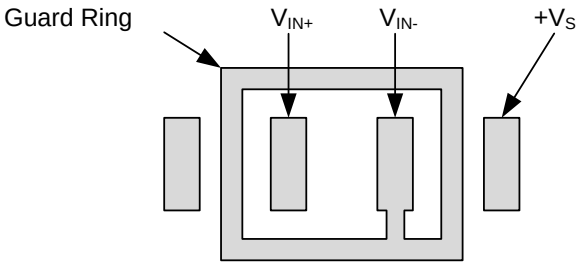
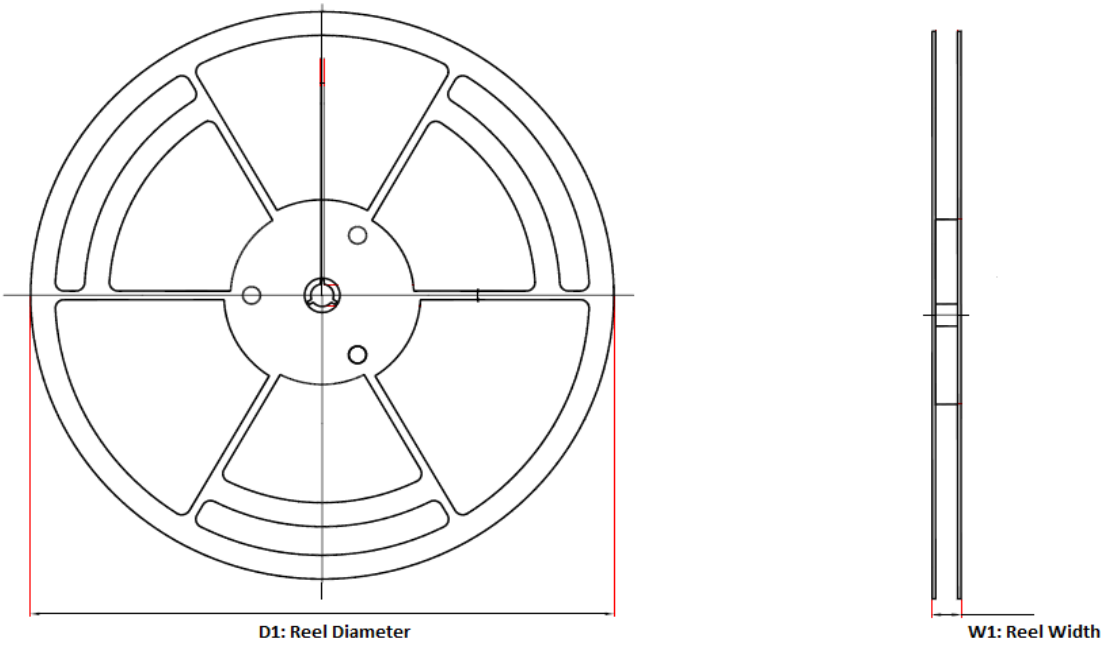


Figure 15 Layout of Guard Ring

Tape and Reel Information

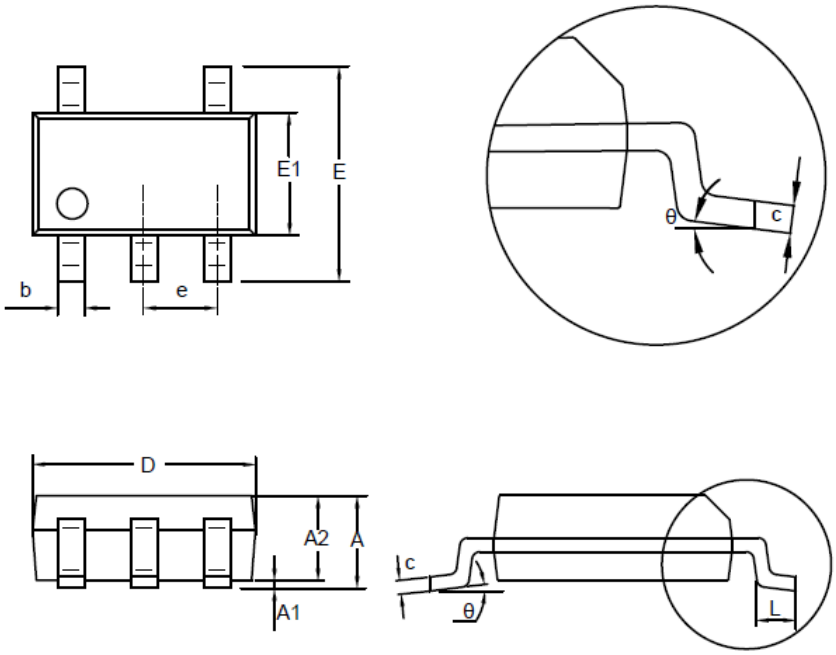


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP5551-SR	SOP8	330.0	17.6	6.5	5.4	2.0	8.0	12.0	Q1
TP5551-TR	SOT23-5	179.0	12.0	3.3	3.25	1.4	4.0	8.0	Q3
TP5552-SR	SOP8	330.0	17.6	6.5	5.4	2.0	8.0	12.0	Q1
TP5552-VR	MSOP8	330.0	17.6	5.2	3.3	1.5	8.0	12.0	Q1
TP5554-SR	SOP14	330.0	21.6	6.5	9.1	2.1	8.0	16.0	Q1
TP5554-TR	TSSOP14	330.0	17.6	6.8	5.5	1.6	8.0	12.0	Q1

Package Outline Dimensions

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



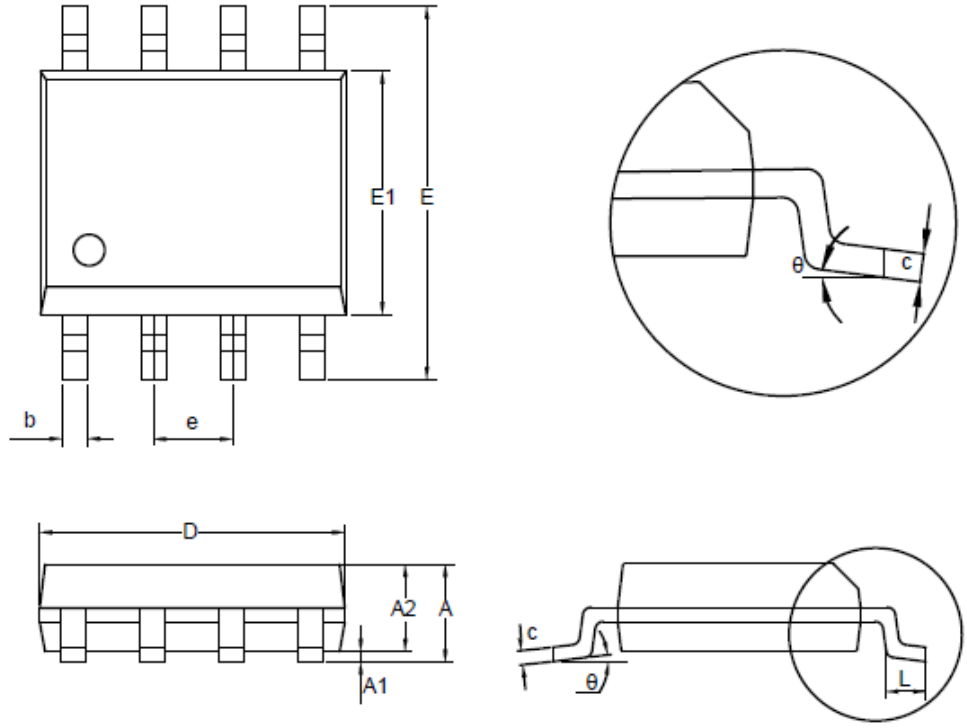
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOP8

Package Outline Dimensions SO1(SOP-8-A)



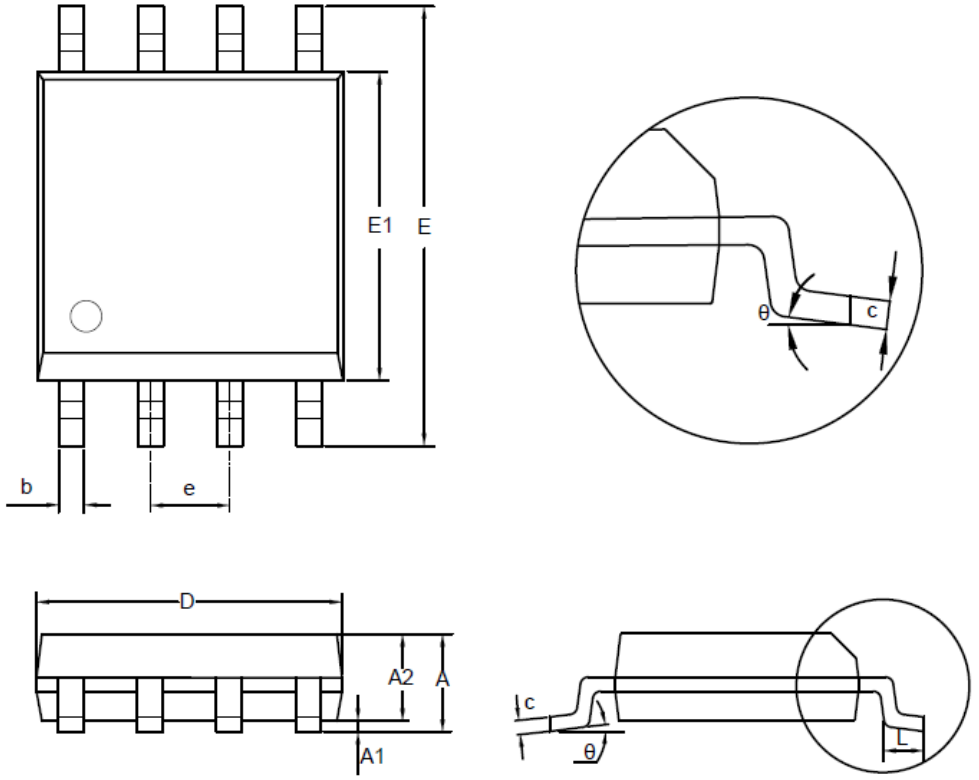
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

MSOP8

Package Outline Dimensions VS1(MSOP-8-A)



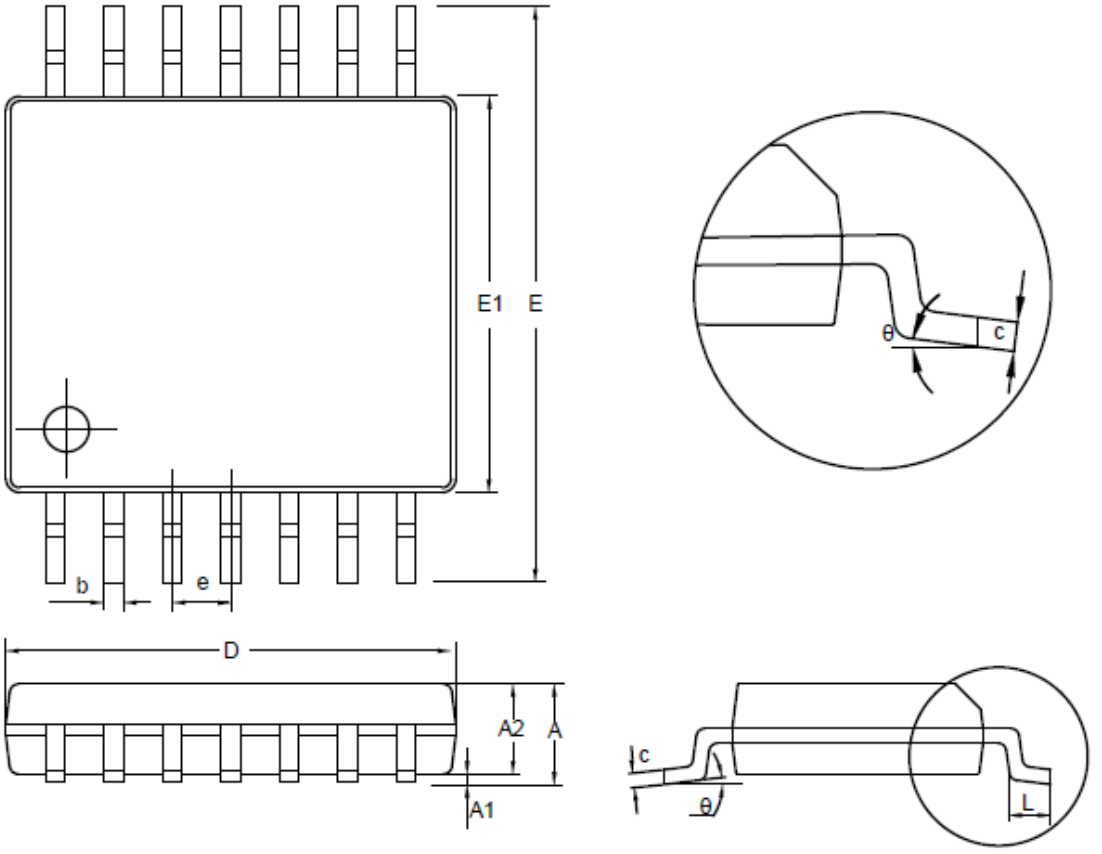
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TSSOP14

Package Outline Dimensions TS2(TSSOP-14-A)



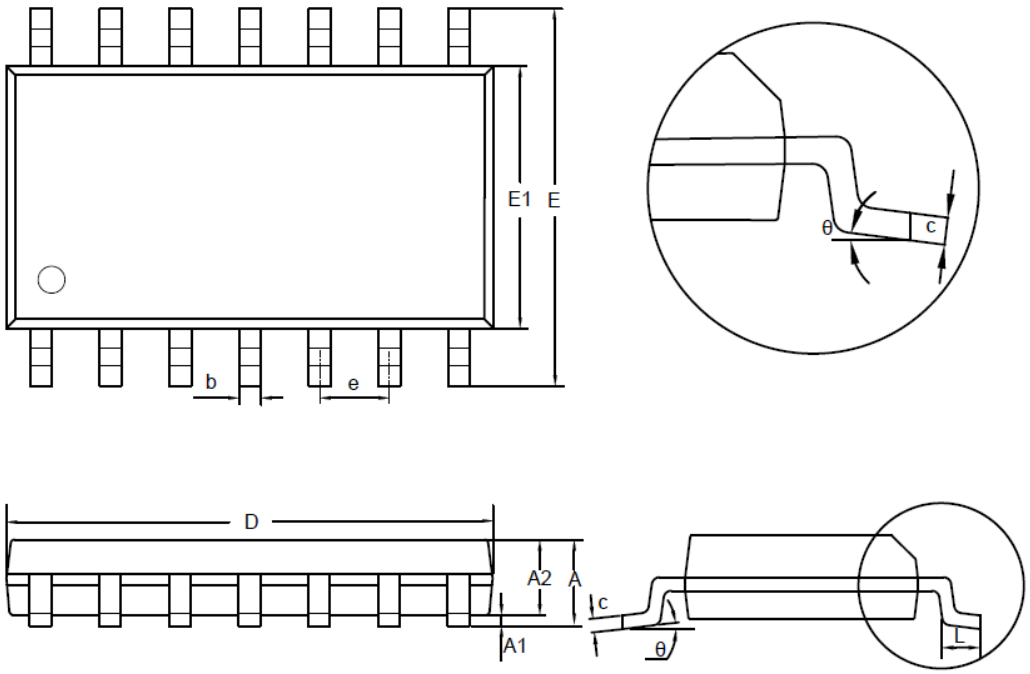
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOP14

Package Outline Dimensions SO2(SOP-14-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TP5551-TR	−40 to 125°C	SOT23-5	E51T	MSL3	Tape and Reel, 3000	Green
TP5551-SR	−40 to 125°C	SOP8	TP5551	MSL3	Tape and Reel, 4000	Green
TP5552-SR	−40 to 125°C	SOP8	TP5552	MSL3	Tape and Reel, 4000	Green
TP5552-VR	−40 to 125°C	MSOP8	TP5552	MSL3	Tape and Reel, 3000	Green
TP5554-SR	−40 to 125°C	SOP14	TP5554	MSL3	Tape and Reel, 2500	Green
TP5554-TR	−40 to 125°C	TSSOP14	TP5554	MSL3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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