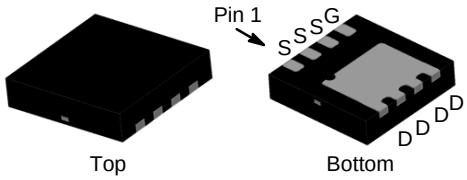
MOSFET – P-Channel, POWERTRENCH®

-150 V, -2 A, 307 mΩ

FDMC86262P

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
−150 V	307 mΩ @ −10 V	−2 A
	356 mΩ @ −6 V	



WDFN8 3.3x3.3, 0.65P
(MLP 3.3x3.3)
CASE 511DH

General Description

This P−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH technology. This very high density process is especially tailored to minimize on−state resistance and optimized for superior switching performance.

Features

- Max $r_{DS(on)}$ = 307 mΩ at V_{GS} = −10 V, I_D = −2 A
- Max $r_{DS(on)}$ = 356 mΩ at V_{GS} = −6 V, I_D = −1.8 A
- Very Low $r_{DS(on)}$ Mid Voltage P−Channel Silicon Technology Optimised for Low Qg
- Optimised for Fast Switching Applications as Well as Load Switch Applications
- 100% UIL Tested
- This Device is Pb−Free, Halide Free and is ROHS Compliant

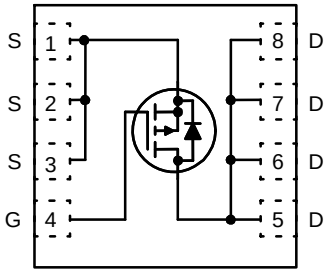
Applications

- Active Clamp Switch
- Load Switch

MARKING DIAGRAM

FDMC86262P = Device Code
&Z = Assembly Plant Code
&K = 2−Digits Lot Run Traceability Code
&2 = 2−Digit Date Code Format

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter			Ratings	Unit
V_{DS}	Drain to Source Voltage			−150	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current	Continuous (Note 3)	T_C = 25°C	−8.4	A
		Continuous (Note 3)	T_C = 100°C	−5.3	A
		Continuous (Note 4a)	T_A = 25°C	−2	A
		Pulsed (Note 2)		−35	
E_{AS}	Single Pulse Avalanche Energy (Note 1)			37	mJ
P_D	Power Dissipation		T_C = 25°C	40	W
	Power Dissipation (Note 4a)		T_A = 25°C	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to +150	°C

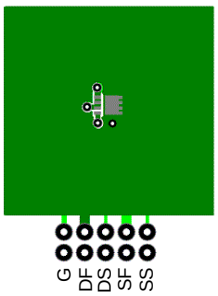
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting T_J = 25°C, L = 3 mH, I_{AS} = −5 A, V_{DD} = −150 V, V_{GS} = −10 V.
2. Pulsed Id please refer to Figure 11 SOA graph for more details.
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

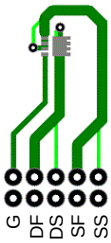
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 4a)	53	

4. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−150	−	−	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	−	−86	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −120 V, V_{GS} = 0 V	−	−	−1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V	−	−	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	−2	−2.9	−4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	−	5	−	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = −10 V, I_D = −2 A	−	241	307	mΩ
		V_{GS} = −6 V, I_D = −1.8 A	−	266	356	
		V_{GS} = −10 V, I_D = −2 A, T_J = 125°C	−	425	541	
g_{FS}	Forward Transconductance	V_{DS} = −10 V, I_D = −2 A	−	5.4	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −75 V, V_{GS} = 0 V, f = 1 MHz	−	632	885	pF
C_{oss}	Output Capacitance		−	45	65	pF
C_{rss}	Reverse Transfer Capacitance		−	1.3	2.0	pF
R_g	Gate Resistance		0.1	3	6	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −75 V, I_D = −2 A, V_{GS} = −10 V, R_{GEN} = 6 Ω	−	8.5	17	ns
t_r	Rise Time		−	2.2	10	ns
$t_{d(off)}$	Turn−Off Delay Time		−	15	26	ns
t_f	Fall Time		−	5.6	11	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to −10 V, V_{DD} = −75 V, I_D = −2 A	−	9.1	13	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to −6 V, V_{DD} = −75 V, I_D = −2 A	−	5.6	7.9	nC
Q_{gs}	Gate to Source Charge	V_{DD} = −75 V, I_D = −2 A	−	2.5	−	nC
Q_{gd}	Gate to Drain “Miller” Charge		−	1.6	−	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source−Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −2 A (Note 5)	−	−0.8	−1.3	V
t_{rr}	Reverse Recovery Time	I_F = −2 A, di/dt = 100 A/μs	−	72	116	ns
Q_{rr}	Reverse Recovery Charge		−	166	266	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED)

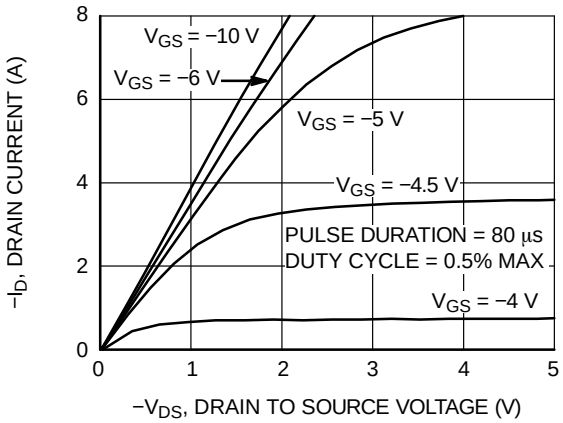


Figure 1. On Region Characteristics

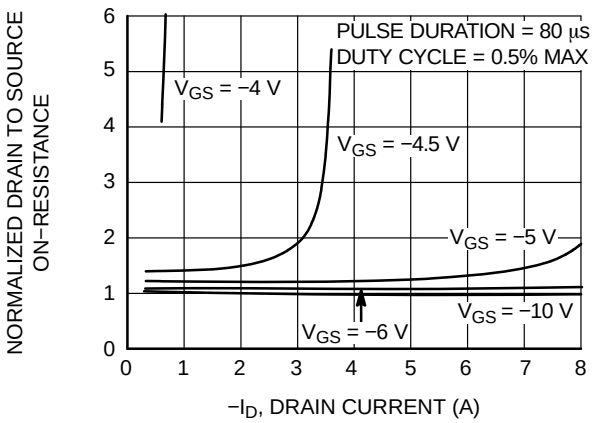


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

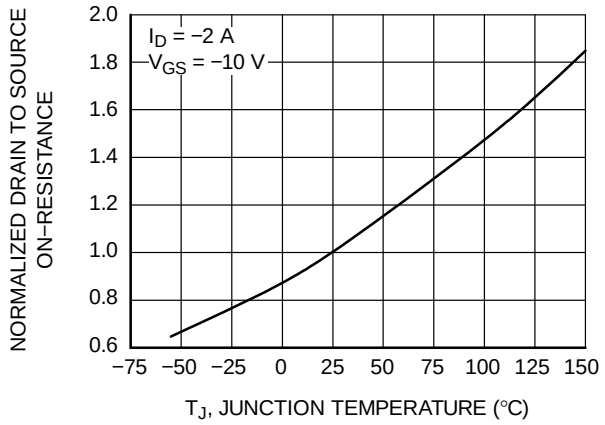


Figure 3. Normalized On−Resistance vs. Junction Temperature

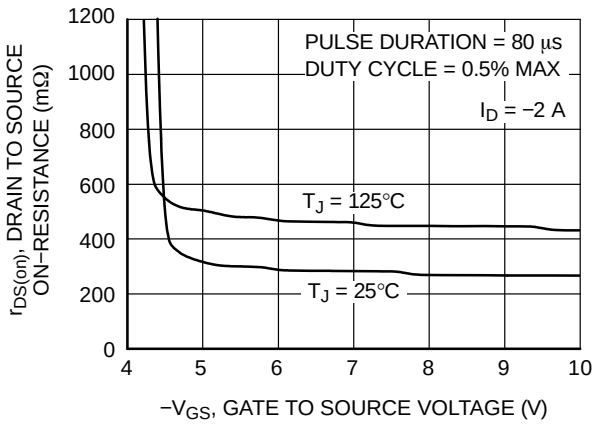


Figure 4. On Resistance vs. Gate to Source Voltage

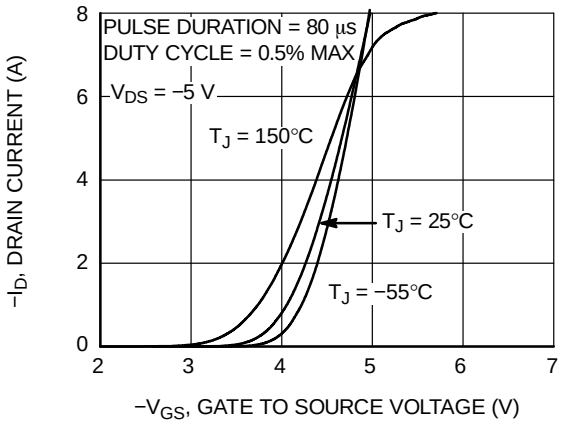


Figure 5. Transfer Characteristics

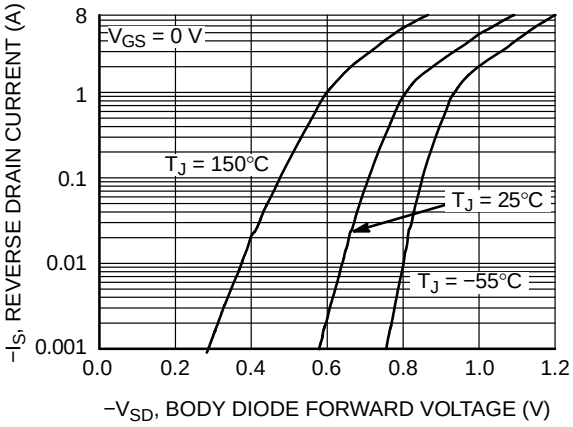


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

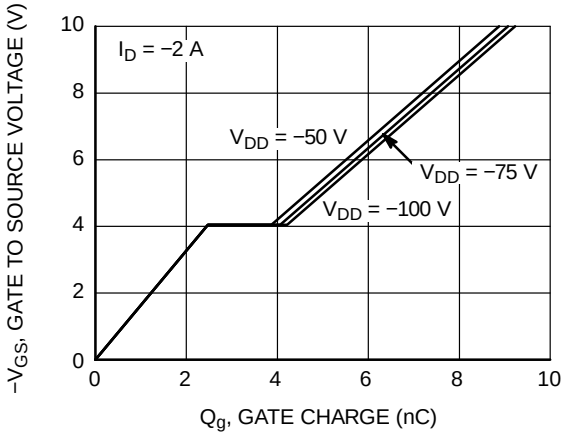


Figure 7. Gate Charge Characteristics

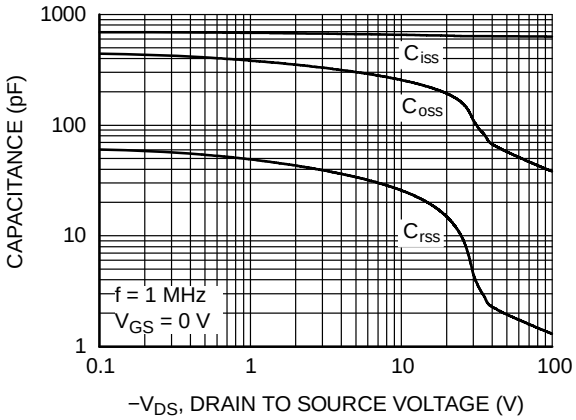


Figure 8. Capacitance vs. Drain to Source Voltage

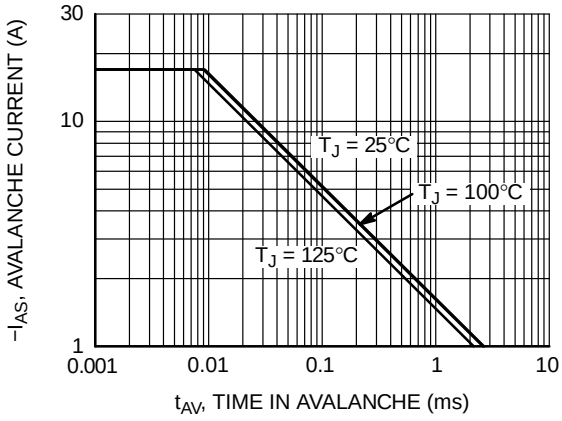


Figure 9. Unclamped Inductive Switching Capability

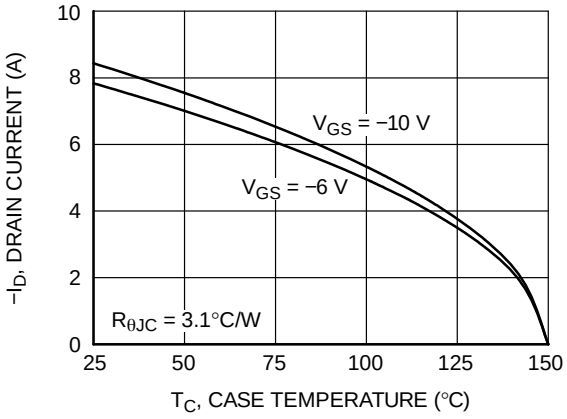


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

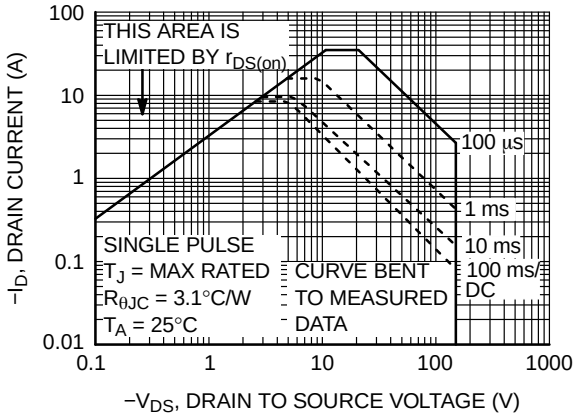


Figure 11. Forward Bias Safe Operating Area

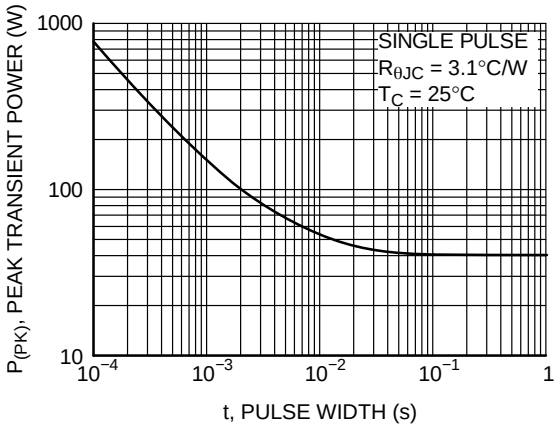


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

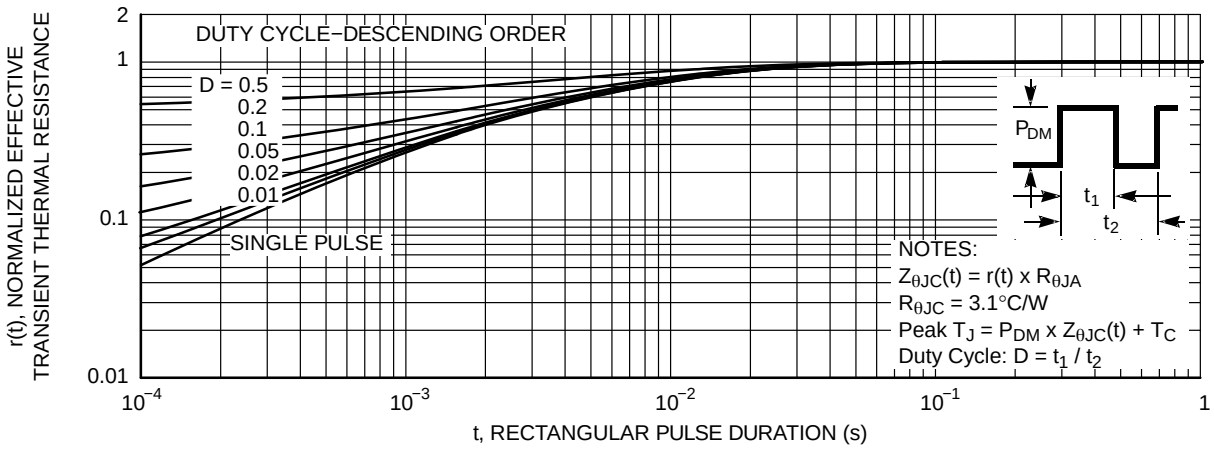


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

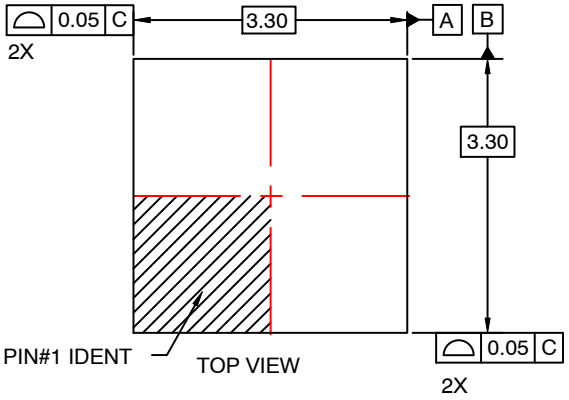
PACKAGE MARKING AND ORDERING INFORMATION

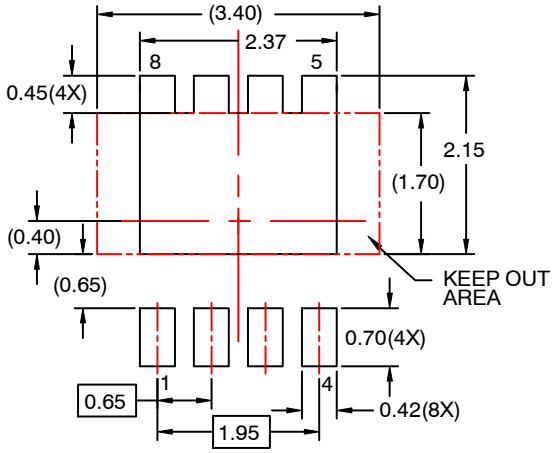
Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDMC86262P	FDMC86262P	WDFN8 3.3x3.3, 0.65P Power 33 (Pb−Free, Halide Free)	13”	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

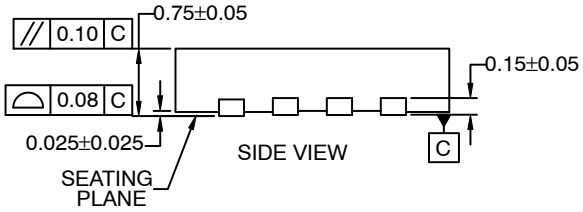
WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

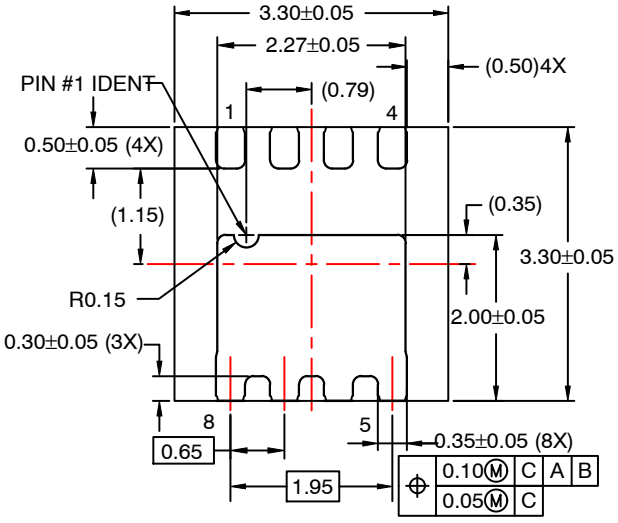
DATE 31 JUL 2016





RECOMMENDED LAND PATTERN





BOTTOM VIEW

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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